

Large Memory Window of van der Waals Heterostructure Devices Based on MOCVD-Grown 2D Layered Ge₄Se₉

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Van der Waals (vdW) heterostructures have drawn much interest over the last decade owing to their absence of dangling bonds and their intriguing low-dimensional properties. The emergence of 2D materials has enabled the achievement of significant progress in both the discovery of physical phenomena and the realization of superior devices. In this work, the group IV metal chalcogenide 2D-layered Ge₄Se₉ is introduced as a new selection of insulating vdW material. 2D-layered Ge₄Se₉ is synthesized with a rectangular shape using the metalcorganic chemical vapor deposition system using a liquid germanium precursor at 240 °C. By stacking the Ge₄Se₉ and MoS₂, vdW heterostructure devices are fabricated with a giant memory window of 129 V by sweeping back gate range of ±80 V. The gate-independent decay time reveals that the large hysteresis is induced by the interfacial charge transfer, which originates from the low band offset. Moreover, repeatable conductance changes are observed over the 2250 pulses with low non-linearity values of 0.26 and 0.95 for potentiation and depression curves, respectively. The energy consumption of the MoS_2/Ge_4Se_9 device is about 15 fJ for operating energy and the learning accuracy of image classification reaches 88.3%, which further proves the great potential of artificial synapses.

1. Introduction

Van der Waals (vdW) heterostructure devices can exert many interesting physical phenomena,^[1-7] such as exciton dynamics,^[8] interfacial charge transfer,^[9,10] and the superconductivity in moiré structures.^[11] Recently, the density functional theory (DFT)-based high-throughput computations have predicted that there are more than a thousand candidate crystals could possibly exist in the form of 2D layered materials (2DLM).^[12] However, fewer than a hundred 2DLM among the candidate materials are available to synthesize. Therefore, there are still many opportunities to discover new 2DLM, and various combinations of vdW heterostructures can be generated from the new 2DLM through vdW stacking. For device applications implementing these vdW heterostructures, the engineering of the band offset that is created at the junction of

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adjacent materials is important,^[2,5,6,13,14] as the optoelectrical properties of the vdW heterostructure device, such as the carrier mobility, subthreshold swing, and recombination rate, can be modulated depending on the range of the band offset.^[15–20] Indeed, the band offset engineering has already been applied to conventional devices, such as the 2D electron gas (2DEG), photodetector, and solar cell.^[21–24] In this regard, establishing the library of the 2D vdW material group serves an indispensable role in not only expanding the band offset spectrum but also bridging the various approaches for device applications beyond fundamental material research.

Meanwhile, the group-IV metal chalcogenide family (group-IV metal = Ge, Sn/chalcogen = S, Se, Te) has been actively reported as a wide bandgap 2D vdW material over the last few years.^[25-27] In particular, the GeSe and GeSe₂ phases exhibited interesting material characteristics,^[28-31] such as magnetism,[32] ferroelectricity,[33,34] thermoelectricity,[35] and nonlinear optics,^[36] and could be potentially used in photonics and electronics applications, including in ovonic threshold switch devices.^[37-40] According to the band structure calculation for the germanium selenide phases, Ge₄Se₉, which has not been reported to grow in 2D vdW form yet, remains an interesting material as it exhibits a small band offset with MoS₂, which is the major channel material for 2D heterostructure devices. This small band offset for the vdW heterostructure device can induce an interfacial charge transfer with a large hysteresis window. As a result, Ge₄Se₉ can be expected to serve as an important building block for the design of vdW heterostructure devices' functions based on band offset engineering, including artificial synaptic devices with a large dynamic range and linear weight tunability.

Here, we report upon the synthesis of the new phase of 2D vdW material, Ge_4Se_9 , by using metal–organic chemical vapor deposition (MOCVD). In order to realize the new phase Ge_4Se_9 growth, which can be stabilized at a low temperature, we designed precursors for MOCVD that can be decomposed at a low temperature with high steric hindrance. To explore the functionality of Ge_4Se_9 , we demonstrated a vdW hetero-structure device with MoS₂ and surprisingly, it showed a giant hysteresis window of 129 V by sweeping a back-gate voltage at

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 ± 80 V in a different direction. Due to the low conduction band offset between MoS₂ and Ge₄Se₉, the interfacial charge transfer was induced, resulting in large hysteresis behavior with linear gate-tunability, which was also verified by the theoretical model and experiment results. Last, in order to exploit the charge transfer of the MoS2/Ge4Se9 vdW heterostructure, we demonstrated bioinspired synaptic behaviors with the device including potentiation and depression curves with excellent non-linearity values ($v_{po} = 0.26$ and $v_{de} = 0.95$). In particular, the long-term plasticity after short-time decay within sub-seconds implies that the MoS₂/Ge₄Se₉ vdW heterostructure device can exert both volatile and non-volatile memory properties, which could be applied to a multifunctional memory related to associative learning.^[41,42] The energy consumption of MoS₂/Ge₄Se₉ vdW heterostructure device as an artificial synapse was estimated to be 15 fJ for updating and 40 fJ for reading energy, which are similar to the typical biological synapse energy consumption per event. Based on the outstanding synaptic device performance, we conducted MNIST handwritten image classification. The learning accuracy reached 88.3%, which is comparable to the ideal case.

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2. Results and Discussion

2.1. Low-Temperature Growth of 2D-Layered Ge₄Se₉

Figure 1a shows the crystal structures of GeSe₂ and Ge₄Se₉, respectively. Ge₄Se₉ is a slightly Se-rich phase compared to GeSe₂, and the two phases have the similar structure in the main frame of GeSe₄ tetrahedral. While GeSe₂ consists of 50% edge-sharing tetrahedral and 50% corner-sharing tetrahedral; by contrast, Ge₄Se₉ consists of only corner-sharing components, as the edge-shared portions of GeSe₂ are changed to Se–Se corner shared components.^[43,44] According to the phase diagram (Figure S1a, Supporting Information),^[43] Ge₄Se₉ decomposes into GeSe₂ and changes into a liquid phase at 385 ± 5 °C, which implies that the Ge₄Se₉ requires a lower temperature than GeSe₂.

Figure 1b shows a schematic of the MOCVD system of the Ge-Se compound. The two-zone heating system in our MOCVD reactor allows us to control the precursor decomposition at the first heating zone (T_1) and separately synthesize the crystal at the second heating zone (T_2) . Ge(dmamp)₂ and dimethyl selenide (CH₃)₂Se were used as Ge and Se precursors, respectively, while muscovite mica served as the substrate. We maintained the T_1 of 480 °C in order to decompose the precursors, and adjusted the temperature of T_2 to manipulate the phase of the Ge-Se compound: a high temperature of 400 °C for GeSe₂ and a low temperature of 240 °C for Ge₄Se₉. The change in the morphology of the Ge-Se compound can be observed from Ge₄Se₉, which comes in the form of a rectangular shape, all the way to GeSe2, which forms a rhombus shape at the range of temperature of T_2 from 240 to 400 °C, as shown in Figure S2, Supporting Information.

First, we characterized our Ge_4Se_9 , grown at a T_2 temperature of 240 °C. The optical reflectance image in Figure 1c shows that Ge_4Se_9 has thin 2D crystals with a rectangular shape with sharp facets. The flat surface and sharp edges were confirmed www.advancedsciencenews.com



Figure 1. Growth of the Ge–Se compound. a) Crystal structure of GeSe₂ and Ge₄Se₉. The dashed line represents the unit cell of crystal. b) Schematics of the MOCVD method with temperature-dependent Ge–Se phase modulation, (GeSe₂: 400 °C, Ge₄Se₉: 240 °C). c) Optical reflectance image of Ge₄Se₉ flakes on mica substrate. d) AFM image of Ge₄Se₉ with 7 nm height. e) XRD measurement of Ge₄Se₉. The inset shows magnified graph of the (002) peak. f) Raman spectrum of Ge₄Se₉.

by the atomic force microscopy (AFM) image in Figure 1d. The thickness of the as-synthesized flakes ranged from 5 to 50 nm, depending on the conditions of growth temperature and growth time. Figure 1e shows the X-ray diffraction (XRD) pattern of rectangular flakes after the grown Ge₄Se₉ on the mica substrate was dry transferred to a SiO₂/Si substrate. The flake peaks were well matched with the orthorhombic Ge₄Se₉ (JCPDS 01-073-3670)^[44] with a distinct peak (14.67°) belonging to the (002) crystal plane. In addition, the observed group of (001) plane direction peaks indicates that our grown Ge₄Se₉ is well aligned in the *c*-axis directions. Figure 1f shows the Raman spectrum of the as-grown flake. The Raman scattering bands at 198 and 214 cm⁻¹ were due to the Ge-Se bonding, and the scattering band of 260 cm⁻¹ was due to the Se-Se dimer.^[45] The GeSe₂ was grown when the T_2 was heated at 400 °C. The optical reflectance image and the AFM image in Figure S3, Supporting Information, show the uniform distribution of a rhombic structure with a sharp facet. The XRD pattern is consistent with GeSe₂ (JCPDS-01-071-0177), and the prominent peak (210 cm⁻¹) in the Raman spectrum exhibits the out-of-plane A_g mode of GeSe₂.

The Ge₄Se₉ phase was further investigated using transmission electron microscopy (TEM). The orthorhombic structure of the grown material was observed through a selected-area electron diffraction (SAED) pattern and energy-dispersive X-ray spectroscopy (EDX) analyses. **Figure 2**a shows a lowmagnification, high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of the Ge₄Se₉ flake. The high-resolution TEM (HR-TEM) image was shown in Figure S4, Supporting Information, which exhibited a precisely ordered nature without the segregation of different phases or dislocations in the Ge₄Se₉ crystal. The SAED

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Figure 2. Characterizations of few-layer Ge₄Se₉. a) Low-magnification STEM image of Ge₄Se₉, and b) the corresponding SAED pattern. c) Simulated electron diffraction pattern of Ge₄Se₉ taken along the [001] zone axis. d) EDX spectrum obtained from a Ge₄Se₉ in (a). The inset table exhibits the elemental ratio of Ge and Se. The Si and N originated from SiN TEM grid. e) Ge and Se EDX mapping images.

pattern in Figure 2b exhibits sharp diffraction spots, which indicate a single-crystal structure with high crystallinity of the flake. Additionally, the SAED pattern of the TEM result was consistent with the simulated electron diffraction pattern seen in the Ge₄Se₉ crystal structure (Figure 2c). According to the SAED pattern results, the Ge₄Se₉ had an orthorhombic crystal with two orthogonal interlayer d-spacings of 9.0 and 7.018 Å, which can be assigned to the (200) and (010) planes that can be observed along the <001> zone axis. These values were also well matched with the interplanar spacing of Ge₄Se₉. Compared with Figure 2a,b, the long side of the rectangular flake is the [100] direction where the Se-Se bonding exists. The elemental ratio of Ge₄Se₉ was confirmed by the EDX spectrum. In the EDX spectrum of Figure 2d, the Si and N peaks originate from the SiN TEM grid, and the measured ratio of Ge and Se is about 4:9, which is consistent with the stoichiometry of Ge₄Se₉. The uniform distribution of Ge and Se can also be seen in Figure 2e. The binding energy of Ge 3d, Se 3d5/2, and Se 3d3/2 peaks are also indicated in Figure S1b,c, Supporting Information, by X-ray photoelectron spectroscopy (XPS). These peaks indicate the +4 oxidation state of Ge and the -2 oxidation state of Se, and the elemental ratio of Ge and Se by EDX was 29.85:70.15, which is similar to the 4:9 ratio of Ge₄Se₉.^[45] Additionally, we obtained the similar results (31.16:68.84) of the elemental ratio by XPS.

We assume that the kinetics-driven two-zone MOCVD system and the low-reactive precursor enable the synthesis of 2D-layered Ge_4Se_9 . The decomposed germanium precursor migrated to the growth zone through lateral gas flow, and the homogenous nucleation of Ge–Se proceeded under the Si-rich environment. In particular, it can reach the growth zone with lower chemical reaction and, simultaneously, create a Si-rich

environment due to the low reactivity of the precursor.^[46,47] Furthermore, based on phonon-free energy calculation, Ge₄Se₉ is stable at temperatures below 327 °C and GeSe₂ is stable above 327 °C (more details in the Note SI, Supporting Information). Thus, GeSe₂ could be grown at a high temperature of T_2 (400 °C), and Ge₄Se₉ could be grown at a low temperature of 240 °C.

The thickness of Ge_4Se_9 flakes can be controlled by the growth temperature and time of the second heating zone (T_2). As shown in Figure S5, Supporting Information, Ge_4Se_9 became thicker with the increase of either the growth temperature or time, respectively. This is because the dominant thermodynamic reaction with high-saturated reactants at high temperature and sufficient growth reaction time cause Ge_4Se_9 to be thicker. Furthermore, we confirmed that the epitaxial growth of Ge_4Se_9 can be possible in mica substrate, which expands the perspective of the feasibility for wafer-scale single-crystal growth of Ge_4Se_9 (details in Note SII, Supporting Information).

From these results, we successfully synthesized the 2D-layered Ge₄Se₉ within a stable phase based on the low-reactive germanium precursor using the MOCVD system at a low temperature of 240 °C. Through the manipulation of the temperature of the growth zone (T_2), we can induce the phaseselective growth of the Ge–Se compound among GeSe₂ and Ge₄Se₉. Our first successful growth of 2D-layered Ge₄Se₉ suggests a new guide for Ge–Se compound synthesis with easy integration for various 2D materials. Additionally, from the point of view of the thermal budget, the low growth temperature (240 °C) holds another advantage for its compatibility and applicability with other conventional fabrication processes.^[48,49]



2.2. Giant Hysteresis Window of MoS_2/Ge_4Se_9 vdW Heterostructure Device

Using the Ge₄Se₉ as a building block of the vdW heterostructures, we demonstrated MoS₂/Ge₄Se₉ vdW heterostructure devices in Figure 3. First, the MOCVD-grown Ge₄Se₉ was transferred onto a degenerated n-doped Si substrate with a 300 nm SiO₂ layer, followed by stacking the exfoliated multilayer MoS₂ on the MOCVD-grown Ge₄Se₉ flake using the dry transfer method. The details of the device fabrication are further explained in the Experimental Section. A drain voltage (V_{ds}) was applied to the MoS₂ channel, and a back-gate voltage was applied through the SiO₂/Si substrate (Figure S6, Supporting Information). In Figure 3b, the device exhibits typical n-type FET behavior with an on/off ratio of about 105. In particular, the hysteresis window ($\Delta V_{\rm th}$) of our device showed about 66.5 V after sweeping the back-gate voltage in the ±50 V range in a different direction (Figure 3b). To investigate the reliability of the large hysteresis of the MoS₂/Ge₄Se₉ vdW heterostructure device, we compared 12 different devices and confirmed that the average $\Delta V_{\rm th}$ value was 64.5 V at the same sweeping voltage of ±50 V (Figure S7a,b, Supporting Information). It should be noted that the ON/OFF ratio and $\Delta V_{\rm th}$ were still maintained after 4 weeks without significant degradation, and the device exhibited repeatable transfer curves for 300 cycles (Figure S7c,d, Supporting Information). Moreover, the hysteresis window

increased linearly with different sweeping ranges of the backgate voltage, and the maximum value of $\Delta V_{\rm th}$ reached upto 129 V at the ±80 V sweeping range, as shown in Figure 3c. In order to confirm the robustness of the device, we also measured the endurance of the switching process between SET and RESET, as shown in Figure 3d. The current levels of the ON and OFF states were observed to be ~10⁻⁷ to 10⁻¹² A, with +50 V for programming and -50 V for erasing at 0.1 V read voltage, respectively. The device exerted great stability over 2000 switching cycles, while maintaining an on/off ratio of about 10⁵.

In previous studies, the hysteresis behavior of MoS₂ FETs was frequently observed, and it is known that the origin of the hysteresis can be attributed to charge trapping and de-trapping processes. The absorption of H₂O and oxygen molecules from the air at the MoS₂ surface can be one possible reason.^[50-52] In addition, charge trapping or de-trapping at the interface between the MoS₂ and the dielectric layer^[9,10,53-56] or intrinsic defects in MoS₂^[57-59] can also cause hysteresis. To study the origin of the large hysteresis window (129 V at ±80 V sweep range) of our MoS₂/Ge₄Se₉ vdW heterostructure device, we fabricated additional devices-a Ge₄Se₉ channel-only FET device and multilayer MoS₂ channel-only FET device-for use in the control experiments. As shown in Figure S8a,b, Supporting Information, the Ge₄Se₉ channel-only FET device shows an insulator property for the current range below $\approx 10^{-12}$ A. Th indicates that Ge₄Se₉ is not the main channel for current flow in



Figure 3. Electrical characteristics of the MoS₂/Ge₄Se₉ vdW heterostructure device. a) Schematic and optical microscopy image of the MoS₂/Ge₄Se₉ vdW heterostructure device with back gate voltage applied through the SiO₂/n-doped Si substrate. MoS₂ and Ge₄Se₉ are marked by the green and yellow dashed line, respectively. Scale bar of the inset: 10 μ m. b) Transfer curves of the device under the different back gate voltage sweep from ±20 to ±50 V at V_{ds} = 0.5 V. The threshold shift (ΔV_{th}) is about 66.5 V at the ±50 V sweeping range. c) ΔV_{th} changes with different back gate voltage ranges. The gray dashed line is fitted to the linear function. d) Endurance of the device between SET and RESET (V_{bg} = ±50 V) process at V_{ds} = 0.1 V, V_{bg} = 0 V.

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the MoS_2/Ge_4Se_9 vdW heterostructure device. Additionally, the transfer curve of the multilayer MoS_2 channel-only FET device without Ge_4Se_9 exhibits small hysteresis behavior, as shown in Figure S8c, Supporting Information, meaning that the large hysteresis in the MoS_2/Ge_4Se_9 vdW heterostructure device does not stem from intrinsic defects in MoS_2 . Last, we measured the device at the 10 mTorr vacuum condition to investigate the effects of H_2O and oxygen molecules in the air on large hyster-

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effects of H_2O and oxygen molecules in the air on large hysteresis. As shown in Figure S8d, Supporting Information, there are no dominant changes between the air and vacuum conditions, so we can exclude the gas absorption effect.

It is also known that the surface effects, such as the dangling bond on SiO₂, can also be another reason for the origin of hysteresis.^[52–54] In order to confirm that we also fabricated additional top-gate devices: i) a MoS₂/Ge₄Se₉ vdW heterostructure device with h-BN (non-dangling bond 2D material with a wide bandgap (\approx 6 eV) as a gate dielectric layer; ii) a MoS₂/ Ge₄Se₉ vdW heterostructure device without h-BN; and iii) a MoS₂-only device with h-BN as a gate dielectric layer; and then performed the comparison experiments, as shown in Figure S9, Supporting Information. It is worth noting that large hysteresis was still observed in the top-gate h-BN/Ge₄Se₉/MoS₂ device, whereas there was small or no hysteresis in both the MoS₂/Ge₄Se₉ top-gate device and MoS₂/h-BN top-gate device. Additionally, we investigated the effect of Ge₄Se₉ thickness on hysteresis induced by the charge traps through defects in the body of Ge_4Se_9 . We compared with the hysteresis in different thicknesses of Ge_4Se in the range between ≈ 15.51 and 45.06 nm. As shown in Figure S10, Supporting Information, the hysteresis tends to decrease as the thickness of Ge_4Se_9 increases, indicating that the defects in the body of Ge_4Se_9 were not the dominant factor for the large hysteresis behavior. From all these results, we can strongly assume that Ge_4Se_9 plays a key role as a charge trap layer in inducing hysteresis behavior, but not in the defects in the body of Ge_4Se_9 .

Together with the verification of Ge_4Se_9 as a charge transfer layer, we further investigated the mechanism of the charge transfer of the MoS_2/Ge_4Se_9 vdW heterostructure device. From the UV–Vis absorption spectrum, the bandgap of the grown Ge_4Se_9 was measured as 2.7 eV (**Figure 4**a), which is close to the DFT calculation result of 2.5 eV, shown in Figure S17a, Supporting Information. The work function and electron affinity were estimated by UV photoelectron spectroscopy and Kelvin probe force microscopy, respectively, as shown in Figure S17c, Supporting Information and Figure 4a (right). Details of the band diagram characterization of Ge_4Se_9 are further explained in Note SIII, Supporting Information. Figure 4b summarizes the complete band diagram model of the MoS_2/Ge_4Se_9 vdW heterostructure.

When a positive gate voltage is applied, the Ge_4Se_9 band tilts in proportion to the edges of the gate sweep range, and the



Figure 4. Charge-transfer mechanism of the MoS_2/Ge_4Se_9 vdW heterostructure device. a) Estimated bandgap and work function of Ge_4Se_9 . The UV–Vis absorption spectrum and corresponding Tauc plot of the Ge_4Se_9 (left), and the work function mapping by KPFM (right). Inset: the line profile (white) of the work function. b) Band diagram of MoS_2 and Ge_4Se_9 based on KPFM and UPS measurement. c) Schematic of charge-trap mechanism applied positive back gate voltage through band diagram. d) Time-dependence of drain current under the change of V_{bg} from 30 to 80 V ranges with increasing 10 V ($V_{ds} = 0.1$ V). e) Extracted time constant (τ) shown in (b) by the fitting of exponential decay function. f) The change of ΔV_{th} at the temperature range 100–500 K within the range $V_{bg} = \pm 50$ V. The red dashed line denotes the exponential fits.

electrons are then confined to the SiO_2 side of Ge_4Se_9 interface. In this case, there are two possible contributions, which affect charge transfer: thermionic emission and tunneling. Note that the conduction band offset (potential barrier height) between

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 Ge_4Se_9/SiO_2 by thermionic emission (Figure 4c). To determine the dominant contribution of the charge transfer, we designed a simple model and calculated the decay time using the following equation, which has been reported in previous studies:^[9,10]

the MoS₂ and Ge₄Se₉ (≈0.65 eV) is small enough for the elec-

trons to be transferred over and then trapped at the interface of

$$\tau = \frac{a}{vT} \tag{1}$$

where *a* is the thickness of MoS_2 and *v* and *T* are the average velocity of the electrons and the transmission coefficient, respectively. In particular, the transmission coefficient of the thermionic emission (T_{TH}) follows the Boltzmann factor, which is represented by:^[9,10]

$$T_{\rm TH} = \exp\left(-\frac{E_{\rm b} - \varepsilon}{k_{\rm B}T}\right) \tag{2}$$

where $E_{\rm b}$ is the potential barrier height between MoS₂ and Ge₄Se₉ (\approx 0.65 eV), ε is the average energy of electrons, $k_{\rm B}$ is the Boltzmann constant, and *T* is the temperature (300 K) of the system. In terms of the transmission coefficient of tunneling, we referred to the Fowler–Nordheim (FN) tunneling mechanism, as shown in the following equation:^[9,10,60,61]

$$T_{\rm FN} = \exp\left(-\frac{4\sqrt{2m^*}}{3\hbar}\frac{(E_{\rm b}-\varepsilon)^{3/2}t}{eV_{\rm Ge_4Se_9}}\right)$$
(3)

where m^* is the effective mass of electron, \hbar is the Plank constant, t is the thickness of Ge₄Se₉, and $V_{\text{Ge}_4\text{Se}_9}$ is the applied voltage to Ge₄Se₉ at a back-gate voltage level of +50 V. Note that T_{TH} is independent of the applied gate voltage, while T_{FN} is dependent on the applied gate voltage from the above equation. The calculated T_{TH} and T_{FN} are $\approx 3.78 \times 10^{-11}$ and $\approx 1.16 \times 10^{-17}$, respectively (more details in Note SIV, Supporting Information). The difference between the T_{TH} and T_{FN} values was about six orders of magnitude, indicating that the thermionic emission held the dominant effect over the tunneling on the charge transfer between MoS₂ and Ge₄Se₉ in our vdW heterostructure. Additionally, from the value of T_{TH} , we can estimate the decay time of ≈ 1.26 s for the thermionic emission.

In order to experimentally confirm the charge transfer model of the MoS₂/Ge₄Se₉ vdW heterostructure device, we measured the time dependence of the current level by increasing the gate voltage from 30 to 80 V with 10 V steps (Figure 4d), followed by the time constant (7) extraction through the fitting of the exponential decay function, as shown in Figure 4e. The extracted time constant was measured ≈1.5 s, regardless of the applied gate voltage, consistent with the calculated decay time for the thermionic emission (1.26 s). From the temperature dependence measurement of hysteresis behavior, as shown in Figure 4f, the ΔV_{th} exhibited an exponential increase from 100 to 500 K, following

the Boltzmann factor. Simultaneously, the drain ON current level gradually decreased (Figure S11, Supporting Information), which indicates that the electrons of MoS₂ were transferred more to Ge_4Se_9 at a high temperature. From all these results, we can conclude that the large hysteresis window of our MoS₂/Ge₄Se₉ vdW heterostructure device originates from the interfacial charge transfer based on the thermionic emission, owing to the low band offset of MoS_2/Ge_4Se_9 (of ≈ 0.65 eV). It is noteworthy that our MoS₂/Ge₄Se₉ vdW heterostructure device exhibits a lower conduction band offset compared to the other previous reports of the heterojunction between 2D semiconductors and wide-bandgap materials (Figure S12, Supporting Information).^[9,10,55,62-66] Namely, in order for there to be a convenient charge transfer exerting a large hysteresis window, a suitable material configuration for low band offset should be required. In this regard, Ge₄Se₉ can possibly be a novel selection of 2D insulating material for the low-band offset formation of MoS₂ with a type I vdW heterostructure.

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2.3. Potential for Artificial Synaptic Device Application

Thanks to the novel memristive performance of 2D-based memory devices, such as their low energy consumption, flexibility, and high integration, the utilization of 2D-based synaptic devices^[67,68] has been reported in the last few years. Hence, we further investigate the potential use of the MoS_2/Ge_4Se_9 vdW heterostructure as a synaptic device based on the interfacial charge transfer (**Figure 5**a). One of the key factors of a synaptic device is the linear weight update operations, and many studies have reported that low non-linearity is required to achieve a high-performance neuromorphic system.^[69,70]

In order to investigate the use of MoS_2/Ge_4Se_9 vdW heterostructure as a synaptic device, we applied voltage pulses at the back-gate terminal. Figure 5b reveals the gradual changes of post-synaptic current (PSC) at three different back-gate read voltages after applying 32 pulses (potentiation for -22 V with 1 ms and depression for +22 V with 1 ms). For over 2250 cycles, our device exhibited stable and linear conductance modulations for potentiation and depression behaviors. Indeed, in Figure 5c, we obtained the nonlinear values of 0.26 and 0.95 for potentiation and depression, respectively, from the following equations^[70]

$$G_{\rm po} = G_1 \left(1 - e^{\nu P} \right) + G_{\rm min}, \quad G_{\rm de} = G_{\rm max} - G_1 \left(1 - e^{-\nu (P-1)} \right) \tag{4}$$

$$G_{1} = \frac{G_{\max} - G_{\min}}{1 - e^{\nu P}}$$
(5)

where the *v* is the nonlinear value, *P* is the normalized pulse number, G_{max} is the maximum conductance, and G_{min} is the minimum conductance. We believe that the low non-linearity (*v* < 1) could originate from the interfacial charge transfer by the intrinsic low band offset of the MoS₂/Ge₄Se₉. This is because the electrons trapped between Ge₄Se₉ and SiO₂ are dominantly affected by the pulse-induced band bending of Ge₄Se₉. In other words, the number of trapped electrons is proportional to the applied pulse voltage. Indeed, the PSC was linearly increased when the pulse voltage was applied from -5 to -30 V, which indicates that the electrons trapped by pulse-dependent band bending are gradually released (Figure 5d).





Figure 5. Potential for emulating biological synapse. a) Illustration of the synaptic behavior by the artificial memtransistor using the gate terminal for pre-synapse, and source–drain terminal for post-synapse. b) The post-synaptic current (PSC) is modulated by the ±22 V pulse voltage with 1 ms width, corresponding to the potentiation and depression behavior within the 32 states. c) Non-linearity of potentiation and depression curve measured by applying the pulse with ±15 V amplitude and 100 μ s width. d) Changes of PSC with incremental pulse amplitude from –5 to –30 V. e) Retention characteristics of programmed and erased states at $V_{bg} = 0$ V and $V_{ds} = 0.1$ V after applied pulse of +15 and –30 V, 1 ms. f) Time dependence of PSC under the applied five pulses (amplitude; –30 V, 1 ms width, 10 s period). g) MNIST handwritten image classification and the accuracy by setting ideal of parameters and the MoS₂/Ge₄Se₉ vdW device.

The energy consumption for our MoS_2/Ge_4Se_9 synaptic device was estimated to be approximately 15 fJ for updating energy and 40 fJ for reading energy, using the following equation^[71,72]

$$E = V_{\rm spike} \times I \times t_{\rm duration} \tag{6}$$

where V_{spike} is the amplitude of update and read spike, *I* is the current of each operation mode, and t_{duration} is the duration of update and read spike, respectively (Figure S13, Supporting Information).

The retention characteristics of programmed and erased states were measured as shown in Figure 5e. We applied +15

and -30 V with 1 ms pulses in order to set initially programmed and erased states and observed a time-dependent conductance change of each state at $V_{\rm ds} = 0.1$ V with $V_{\rm bg} = 0$ V. During the first few seconds, the programmed and erased states dramatically decayed, and then they entered in saturation states while maintaining their conductance levels. According to the interfacial charge transfer based on thermionic emission, the programmed and erased states should ideally be returned to the same conductance state, as there is no gate voltage that induces a charge transfer. However, interestingly, we obtained separated conductance saturation levels after the program and erase pulses were applied, thus indicating the presence of synaptic

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long-term plasticity behavior. In order to understand this longterm plasticity, we fitted erased states with a biexponential function and extracted two decay time constants of $\tau_1 = 2.5$ s and τ_2 = 9.2 s. From the two different time constants, we assumed that the transferred charges were partially trapped within the Ge and Se vacancies of Ge₄Se₉, which can occur under Serich growth conditions.^[73] According to previous reports,^[9,74] the shorter time constant τ_1 could be affected by the charge transfer, while the longer time constant τ_2 could be related to the vacancies at the body of Ge₄Se₉. This is due to the vacancy energy states present within Ge₄Se₉ bandgap having a higher potential barrier than the conduction band offset of the heterostructure. The presence of both short-term and long-term characteristics was still maintained after applying multiple pulses. Figure 5f shows the time-dependence of PSC after 5 pulses with 1 ms width and 10 s period for each pulse when the decay process was progressed considerably. After five consecutive pulses were applied, the saturated PSC clearly exhibits a different state from the original state. Moreover, both the excitatory and inhibitory states of the long-term plasticity were obtained for 1000 s (Figure S14, Supporting Information). Thus, our MoS2/Ge4Se9 vdW heterostructure device exhibited both volatile (short-time decay in the subsecond range) and nonvolatile (long-term plasticity after a few seconds) behaviors that can be further exploited in artificial learning systems, such as associative learning.[41,42,52]

Finally, we performed the MNIST handwritten image classification in order to expand the utility of the Ge₄Se₉ synaptic device. The multilayer perceptron (MLP) simulation was designed by the two-layer of MLP neural network consisted of 400 input neurons (MNIST handwritten image; 20×20 pixels), one hidden layer with 100 neurons (the simplified input features based on synaptic weight matrix), and ten output neurons (corresponding to the numbers from 0 to 9) as shown in Figure 5g. Each layer of neurons was fully connected by the synapses, and the weights of synapses were updated through the feed-forward and back-propagation processes.[69,75-78] The device parameters for the synaptic array in the simulation were selected from the several PD curves (80 states) measurement results with relatively high dynamic range $(G_{\text{max}}/G_{\text{min}})$ of around 4 with low linearity. For the neural network training, each epoch used 8000 images randomly selected from 60 000 training data set by using the Adam algorithm. After the training, the image classification accuracy was evaluated by 10 000 images from the test data set. As shown in Figure 5g, the learning accuracy was achieved and reached a maximum of 88.3% (average of 86.17%), which is comparable to the 93.85% of the ideal case.

3. Conclusion

We have successfully developed a new 2D material growth method, specifically for 2D-layered Ge_4Se_9 . We expect that the precursor engineering that we used to grow 2D-layered Ge_4Se_9 could provide a general route to achieve a new 2DLM. Furthermore, owing to the non-dangling bond of 2D materials, the configuration of the vdW heterostructure with semiconductor and insulator has been one of the most attractive candidates exhib-

iting high device performance, such as mobility, subthreshold swing, and memory window. In this regard, Ge₄Se₉ offers a new type of 2D insulating material family by offering various heterostructure configurations. Specifically, due to the intrinsic low-conduction band offset, the MoS₂/Ge₄Se₉ vdW heterostructure device exhibits a large hysteresis window (129 V at ±80 V back-gate sweep) with linear gate-tunability and also applicability to a synaptic device with low non-linearity ($v_{po} = 0.26$ and $v_{de} = 0.95$), the low energy consumption (15 f) for updating energy), and also high learning accuracy (88.3%). Therefore, we believe that Ge₄Se₉ can provide remarkable opportunities for band offset-related applications, in addition to neuromorphic research.

4. Experimental Section

MOCVD Growth of GeSe₂ and Ge₄Se₉: The GeSe₂ and Ge₄Se₉ flakes were grown by the MOCVD process, and a tube furnace with a tube diameter of 2 inches was used. Additionally, Ge(dmamp)₂ and (CH₃)₂Se were used as Ge and Se precursors, respectively. (CH₃)₂Se was kept in a bubbler system at a constant pressure of 800 Torr, and Ar was used as the carrier gas. Due to the relatively low vapor pressure, Ge(dmamp)₂ was directly injected into the inlet of the tube by inserting with Ar gas. The canister that contained Ge(dmamp)₂ was kept at 45 °C with the use of heating tape, and the line from the canister to the inlet was also heated. The flow rate was precisely controlled by Mass flow controller. The optimum flow rate of precursor was 60 sccm for Ge(dmamp)₂, 0.6 sccm for $(CH_3)_2Se$, 180 sccm for Ar, and 5 sccm for H_2 , with H_2 also being used to eliminate carbon residue. The tube furnace consisted of two heating zones, and the precursors were decomposed in the first heating zone. The growth of Ge₄Se₉ took place in the second heating zone. Freshly cleaved muscovite mica substrates were placed at the start of the second heating zone, and both heating zones were heated to $T_1 = 480$ °C and $T_2 = 240$ °C (or 400 °C for GeSe₂) for 30 min with Ar 50 sccm and H₂ 10 sccm, with their temperatures maintained during the growth time, and the pressure continuously maintained at around ≈300–400 Torr.

Transfer and Device Fabrication Method: The transfer was done using PDMS and PC. The PC was dissolved in chloroform at a concentration of 5 wt%. The PC was spin-coated at 4000 rpm for 30 s on a mica substrate with Ge₄Se₉ flakes. The PC-coated mica edge was cut with a razor blade to allow water to penetrate effectively in a later step. PDMS was attached to the PC-coated mica substrate to assist the PC films. Afterward, the distilled water was injected by pipette to the side of the sample (PDMS/ PC/Ge₄Se₉/mica). This weakened the adhesive force between mica and the PC/Ge₄Se₉ layer, so the PDMS/PC/Ge₄Se₉ layer to be peeled off from the mica substrate. To attach the sample to the target substrate, the heat was applied to 150 °C while pressing, and the PDMS was then peeled off. PC film was removed through immersion in chloroform, acetone, and IPA, in sequence. In order to fabricate the bottom gate MoS₂/Ge₄Se₉ vdW heterostructure device, exfoliated MoS₂ was used, and Ge₄Se₉ flakes were transferred by way of PDMS/PC-based transfer, and SiO₂ (300 nm)/Si (n⁺⁺) substrate was used. The source and drain were patterned using e-beam lithography (VEGA3 LMH Elphy Quantum Lithography System), and Cr 10 nm Au 40 nm was deposited by e-beam evaporator (SNTEK).

Characterization and Electrical Measurements: Optical microscopy (Olympus) was used to characterize the morphology of Ge₄Se₉. Atomic force microscopy (AFM) (Innova-Labram HR800) with the tapping mode was then used to further characterize the morphology and measure the thickness of Ge₄Se₉ flakes. XRD (SmartLab) pattern was obtained with Cu–K α radiation in order to identify the phase and crystallinity. TEM (Titan Cube G2 60–300, Thermo Fisher Scientific) characterization was performed to obtain the SAED pattern, STEM images, and EDX spectrum. Through XPS analysis (Axis-Supra), an atomic bonding state





was obtained. In order to get the Raman spectrum, Raman spectrometry (ARAMIS) was applied with the 514 nm laser. All electrical measurements of the fabricated devices were performed by Keithley 4200A-SCS. Finally, the work function was measured by KPFM with Pt/Ir coated Si tip at the ambient condition. In order to prevent contact with the step of the sample, the scanning process was completed in very low speed mode (\approx 0.1 Hz)

DFT Calculation Method: The density-functional theory (DFT) calculations were performed as implemented in the Vienna Ab initio Simulation Package (VASP) code.^[79] The projector-augmented wave pseudopotentials $[^{80,81]}$ and a kinetic energy cutoff of 500 eV were applied. The Perdew, Burke, and Ernzerhof functional within the generalized gradient approximation was used for the exchange correlation functional.^[82] The long-range van der Waals interaction was described with the vdW-D2 corrections proposed by Grimme in phonon calculations.^[83,84] The primitive 52-atomic orthorhombic unit cell of Ge₄Se₉ with a Γ -centered 2 × 5 × 3 *k*-point mesh and the primitive 48-atomic monoclinic unit cell of $GeSe_2$ with a $\Gamma\text{-centered}$ 5 \times 2 \times 3 k-point mesh were used for the Brillouin zone (BZ) summation. The Hellmann–Feynman forces were relaxed to lower than 0.001 eV $\text{\AA}^{-1}.$ For the band structure calculation, the hybrid functional of Heyd-Scuseria-Ernzerhof, with a mixing parameter of 0.25 and a screening parameter of 0.2 $Å^{-1}$, was used for the exchange–correlation energy of the electrons.^[85] The phonon calculations were performed using Phonopy code.^[86] The dynamical matrix was constructed using the finite-difference method with the Hellmann–Feynman forces calculated within $1 \times 2 \times 1$ supercell for Ge_4Se_9 and $2 \times 1 \times 1$ supercell for $GeSe_2$. The total energies were minimized in self-consistent calculations to lower than 10⁻⁸ eV in order to obtain a high accuracy of the forces. In thermodynamic calculations, an Γ -centered 6 \times 12 \times 6 *q*-point mesh for Ge₄Se₉ and a Γ -centered $12 \times 6 \times 6$ *q*-point mesh for GeSe₂ were used for the BZ summation.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

Keywords

charge transfer, germanium selenide, metal-organic chemical vapor deposition, synaptic devices, van der Waals heterostructures

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