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LETTER

Growth of Tin Halide Perovskite Film on Two-Dimensional Hexagonal Boron Nitride via Thermal Evaporation

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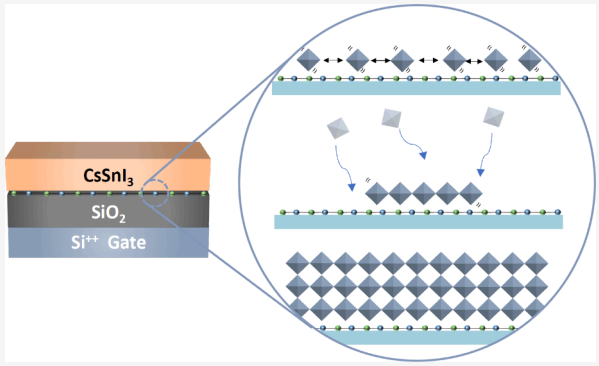
ABSTRACT: Tin halide perovskites have served as channel materials for p-type transistors owing to their low hole effective mass and suitable hole density. However, they suffer from uncontrolled film crystallization, leading to excessive tin vacancies and self-p-doping. In this study, we report a facile way to grow three-dimensional (3D) tin halide perovskite films by thermal evaporation on a dangling-bond-free hexagonal boron nitride (hBN) surface. The hBN, transferred onto SiO_2 as a gate dielectric/channel interlayer, offers a hydrophobic surface that promotes the crystallization of $CsSnI_3$ films by reducing the nucleation site density, increasing the nuclei size, and promoting the formation of uniformly oriented enlarged grains. $CsSnI_3$ films grown on hBN exhibit reduced pinholes and grain boundaries, reducing the concentration of tin vacancies. Thin-film transistors using these films demonstrate accelerated charge transport with large current modulation without any additives. The proposed strategy can facilitate the engineering of defect-free perovskite channel layers for integrated perovskite electronics.



Halide perovskites have emerged as promising candidate materials for solar cells, light-emitting diodes, and photodetectors owing to their exceptional optoelectronic properties, such as high absorption coefficients, tunable bandgaps, and efficient charge transport.[1−9] Tin halide perovskites, as lead-free alternatives, represent high-performance channel materials for p-type transistors owing to their low hole effective mass and suitable hole density arising from the low formation energy of positively charged tin vacancies (V_{Sn}).[10−12] However, this self-doping effect induced by V_{Sn} requires careful modulation for transistor performance. Various approaches, such as chemical composition tuning, additive engineering, and device engineering, have been proposed for V_{Sn} passivation, achieving performances comparable to those of commercialized channel semiconductors.[11−24] Despite these advances, solution-processed tin halide perovskites often suffer from poor crystallinity owing to the high Lewis acidity of Sn^{2+}, forming pinholes and rough surfaces.[13,25−29] To mitigate this, Lewis-based adducts, such as dimethyl sulfoxide, are incorporated to decelerate crystallization.[27,30−34] However, this approach is limited to solution processes. For more scalable and reproducible manufacturing, thermal evaporation offers a promising alternative for forming tin halide perovskite films as transistor channel layers.

The crystallization kinetics of thermally evaporated tin halide perovskites differ from those of solution-processed films, requiring distinct approaches to control film crystallization and quality. Unlike solution processes, which involve solvents that dissociate precursors into ionic species, thermal evaporation uses coevaporated or sequentially evaporated precursor compounds that undergo solid-state reaction during post-annealing.[35,36] Reo et al. demonstrated that incorporating a lead chloride additive layer can help modulate hole concentration and catalyze perovskite phase formation via Cl-related vaporization, yielding highly crystalline films with field-effect mobility exceeding 30 $cm^2 V^{-1} s^{-1}$.[37] However, the role of the growth surface in determining the crystallinity and

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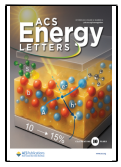

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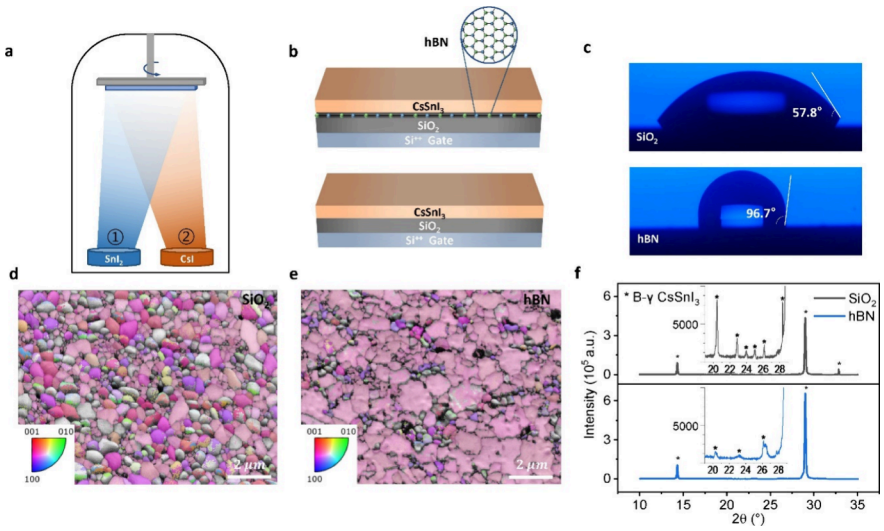

Figure 1. (a) Schematic of thermally evaporated $CsSnI_3$ film. (b) Schematic of $CsSnI_3$ film grown on SiO_2 (bottom) and hBN (top). (c) Water contact angle images of SiO_2 and hBN substrates. Electron backscatter diffraction inverse pole figure maps of $CsSnI_3$ film grown on (d) SiO_2 and (e) hBN. Scale bar, 2 μm. (f) X-ray diffraction pattern of $CsSnI_3$ film grown on SiO_2 and hBN.

electrical performance of the overlying perovskite films remains largely unknown, and an effective interface engineering strategy has yet to be developed.[33,38−40]

Oxide films, such as silicon oxide (SiO_2) films, which are commonly used as dielectric layers, contain dangling bonds on their surfaces. Consequently, they not only introduce abundant interfacial defects but also promote the nucleation of randomly aligned grains, thereby reducing the crystallinity of the channel layer.[41,42] On the other hand, atomically thin layered materials without dangling bonds, such as graphene, offer ideal growth templates and have been used to produce freestanding components of high crystallinity, including perovskites.[43−45] In particular, insulating hexagonal boron nitride (hBN) monolayer films can be integrated into device architectures with minimal geometric perturbations, enabling direct deposition of perovskite films onto the device platform. However, the use of hBN films as interlayers and growth surfaces to enhance the electrical performance of the perovskite channel remains limited.[46]

This paper introduces a facile strategy to achieve highly controlled three-dimensional (3D) tin halide perovskite films by thermal evaporation on a dangling-bond-free hBN monolayer, integrated into device architectures. The resulting polycrystalline $CsSnI_3$ films exhibit uniformly oriented, enlarged grains without pinholes. In addition, these films display low interfacial trap density owing to the formation of a defect- and air-gap-free interface on hBN. The in-plane charge transport properties of $CsSnI_3$ are investigated using thin-film transistors (TFTs). The $CsSnI_3$/hBN TFTs exhibit typical p-type operation, with rational mobility and suitable on/off ratios without requiring additional additives for hole suppression. Thus, the proposed strategy can enable successful operation of 3D tin halide perovskite TFTs without hole suppressors, independent of the deposition technique.

The 40 nm-thick $CsSnI_3$ films were fabricated by sequentially evaporating SnI_2 and CsI precursors onto two substrates, i.e., a 300 nm SiO_2/Si^{2+} wafer and monolayer hBN/300 nm SiO_2/Si^{2+} wafer, followed by postannealing at 180 °C for 10 min. These samples are referred to as SiO_2 and hBN (Figure 1a, b). From XPS analysis, the $CsSnI_3$ film was composed of $CsSnI_{2.9}$, comparable to the ideal 1:1:3 stoichiometric ratio. Monolayer hBN films were epitaxially synthesized on Ge(110) and subsequently transferred onto SiO_2 dielectric, following previously reported methods (see Methods for more details).[47,48] The hydrophobicity of the hBN layer was confirmed through water contact angle measurement on SiO_2 and hBN. The contact angle increased from 57.8° (SiO_2) to 96.7° (hBN) (Figure 1c). The high hydrophobicity of the hBN surface reduced adhesion and interaction between the substrate and deposited material and facilitated precursor diffusion, resulting in growth of films with large grains.[49−52]

Moreover, the substrate polarity can influence the growth orientation of tin halide perovskite crystal lattices. Electron backscatter diffraction (EBSD) was used to map the orientation of the perovskite film, specifically through inverse pole figure (IPF) mapping along the normal direction (z-axis) for $CsSnI_3$ films grown on SiO_2 and hBN (Figure 1d, e). $CsSnI_3$ films grown on SiO_2 exhibited small grains with various orientations, whereas those grown on hBN displayed larger grains with more uniform orientation. The dominant orientation on hBN was (101), indicated in pink, whereas films grown on SiO_2 exhibited mixed orientations of (101), (010), and (110), indicated in pink, green, and yellow, respectively. IPF maps along the rolling and transverse directions (x- and y-axes, respectively) showed similar trends (Figure S1). In addition, EBSD pole figures demonstrated that films grown on SiO_2 had weaker signal intensity and broader signal distributions than those grown on hBN, suggesting enhanced crystallinity (Figure S2). These findings are consistent with the X-ray diffraction (XRD) patterns of $CsSnI_3$ films grown on SiO_2 and hBN (Figure 1f). Both films displayed B-γ-$CsSnI_3$ phase peaks with dominant intensity in (101) and (202) directions at 14.3° and 29.0°, respectively. The film on SiO_2 exhibited weaker XRD peak intensities and additional minor peaks. These include the (103) peak of $CsSnI_3$ at 32.8°, as well as several sharp peaks visible in the inset at angles of 20.4° (121), 22.9° (201), 24.0° (211), 25.0° (220), 26.1° (131), and 28.3° (040). In contrast, the film on hBN showed fewer minor peaks with weaker

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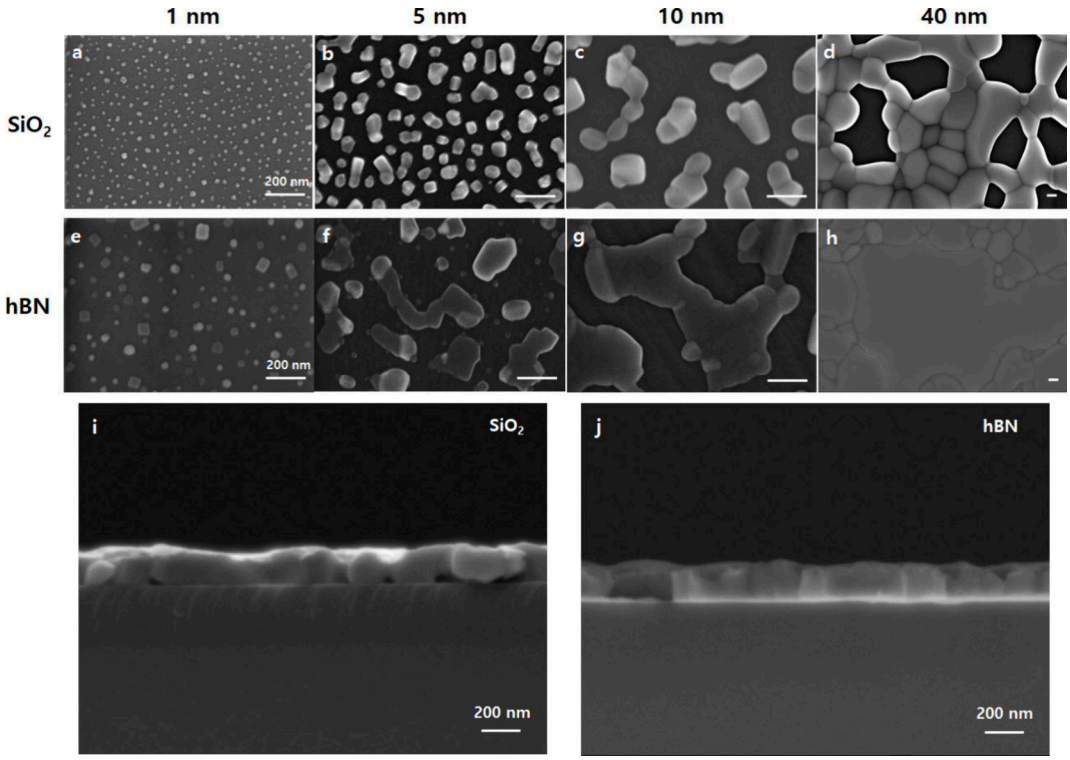

Figure 2. Scanning electron microscopy (SEM) images of $CsSnI_3$ films grown on SiO_2 with increasing film thickness: (a) 1 nm, (b) 5 nm, (c) 10 nm, and (d) 40 nm. SEM images of $CsSnI_3$ films grown on hBN with increasing film thickness: (e) 1 nm, (f) 5 nm, (g), 10 nm, and (h) 40 nm. Cross-sectional SEM images of 200 nm $CsSnI_3$ films grown on (i) SiO_2 and (j) hBN. Scale bar, 200 nm.

intensities. These XRD results are consistent with the EBSD results, verifying that the $CsSnI_3$ crystal lattice orientation is more uniform on hBN than on SiO_2.

To investigate the growth mechanism of $CsSnI_3$ films on SiO_2 and hBN, the film morphologies were analyzed at different film thicknesses (1−40 nm). $CsSnI_3$ films were fabricated by sequentially evaporating SnI_2 and CsI in a 1:1 molar ratio, followed by annealing at 180 °C for 10 min. At a thickness of 1 nm, the film on SiO_2 showed a higher nucleation density than that on hBN (Figure 2a−d). As the film thickness increased, the $CsSnI_3$ film on SiO_2 developed high-density nuclei that coalesced into small grains with similarly sized pinholes.[53] In contrast, the film on hBN initially showed fewer nucleation sites, which transformed into larger grains with fewer grain boundaries and pinholes (Figure 2e−h).[54] To observe the interface properties between $CsSnI_3$ and the substrate, cross-sectional SEM images were obtained (Figure 2i, j). The $CsSnI_3$ film on hBN displayed a perfect interface, with vertically aligned and densely packed grains without air gaps. In contrast, the film on SiO_2 exhibited mixed orientations of crystallites with interfacial voids from pinholes and grain boundaries.

Furthermore, we assessed the atomic diffusion of the as-evaporated CsI and SnI_2 precursors using two-dimensional secondary ion mass spectroscopy (SIMS). We utilized 40 nm-thick $CsSnI_3$ films on hBN and SiO_2 substrates at room temperature (as-deposited, Figure S3) and at highly elevated temperature (320 °C for 10 min, Figure 3a, c) to visually and quantitatively detect a clear difference in diffusivity.[55] We quantified the relative atomic counts along the annotated regions (Figure 3b, d). Ideally, the distribution of the relative number of atoms over distance should follow the blue line in the inset of Figure 3b: zero within the masked region and a constant linear distribution in the unmasked region, indicating the uniform distribution of $CsSnI_3$ in only the unmasked regions. Notably, the as-evaporated $CsSnI_3$ films on both SiO_2 and hBN displayed higher atomic counts at the edge owing to the shadow mask effect, where precursors are concentrated at the shadow mask edges. This surplus at the edge is mitigated after postannealing, and the atomic distribution changes from a vertical profile to a curved gradient, indicating thermal diffusion of the precursors.

The standard deviation values (σ^2) of the number of atoms relative to the center of the region were calculated for as-evaporated $CsSnI_3$ films on SiO_2 and hBN (2.39×10^{-5} cm^2 and 2.58×10^{-5} cm^2, respectively) and annealed $CsSnI_3$ films on SiO_2 and hBN (3.95×10^{-5} cm^2 and 5.19×10^{-5} cm^2, respectively). The as-evaporated film on hBN showed slightly increased σ^2 values, indicating more atomic diffusion on hBN compared with that on SiO_2 at room temperature. Further increase in σ^2 was observed in the annealed films, where more active atomic diffusion of CsI and SnI_2 precursor compounds occurred on hBN than on SiO_2.[56,57] Furthermore, we calculated the mean square displacement of Cs atoms for annealed $CsSnI_3$ films on SiO_2 and hBN (1.67×10^{-5} cm^2 and 3.01×10^{-5} cm^2, respectively). The respective diffusion coefficients were 1.39×10^{-8} cm^2 s^{-1} and 2.51×10^{-8} cm^2 s^{-1}.[56] The higher diffusion coefficients on hBN suggest more active diffusion of CsI and SnI_2 compounds, attributable to the dangling-bond-free and hydrophobic nature of the hBN surface. These behaviors are illustrated in Figure 3e, f. The dangling bonds of SiO_2 serve as nucleation seed points, lowering the nucleation activation energy, accelerating crystallization, and promoting the formation of small grains, as observed in solution processes.[41,58,59] Moreover, these dangling bonds can impede precursor compound diffusion

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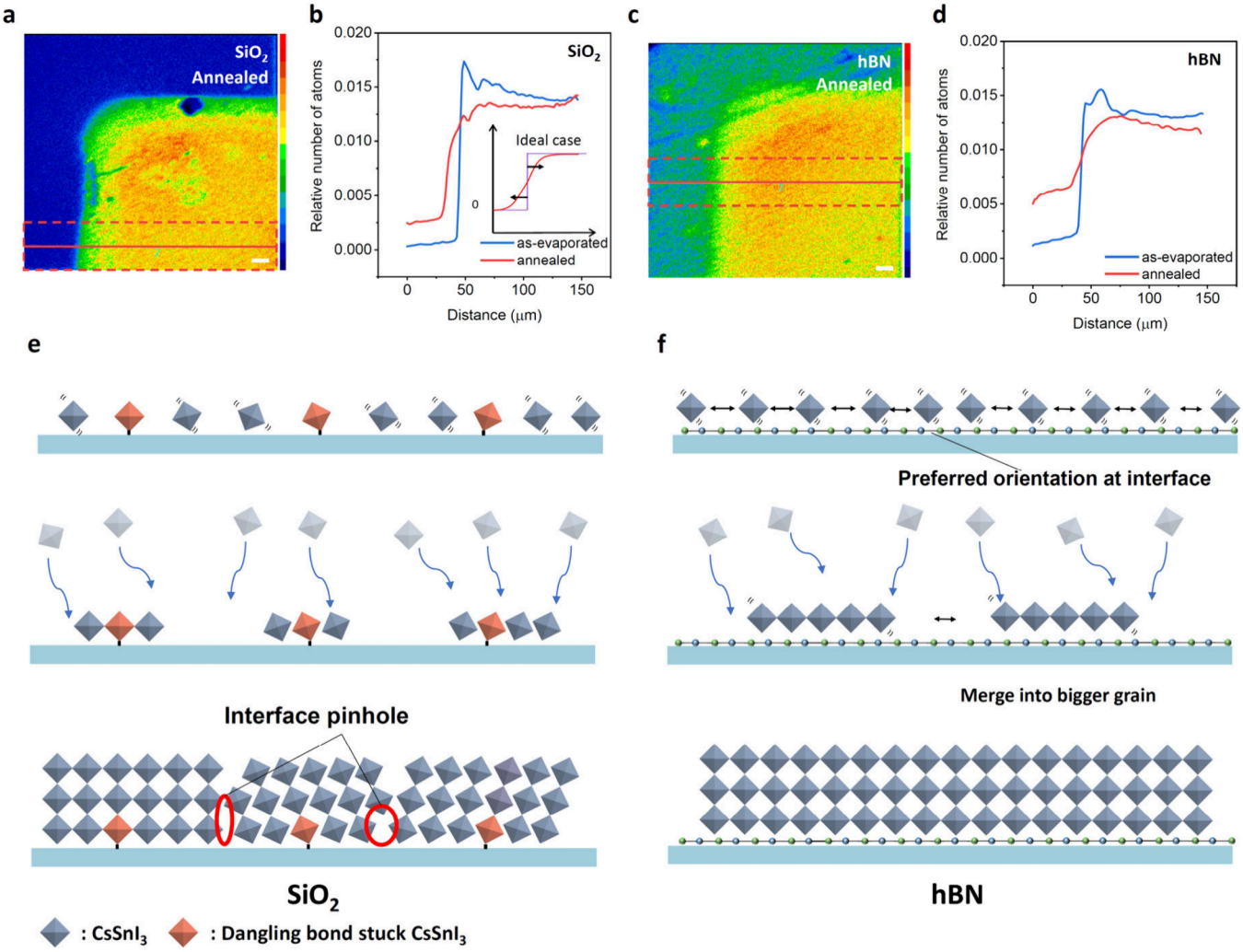

Figure 3. Two-dimensional secondary ion mass (SIMS) spectroscopy images of (a) annealed $CsSnI_3$ films grown on SiO_2. (b) Relative number of atoms over distance following the square areas on each SIMS image of $CsSnI_3$ films grown on SiO_2. SIMS spectroscopy images of (c) annealed $CsSnI_3$ films grown on hBN. (d) Relative number of atoms over distance following the square areas on each SIMS image of $CsSnI_3$ films grown on hBN. Scale bar, 10 μm. Schematic of thermally evaporated $CsSnI_3$ film lattice growth on (e) SiO_2 and (f) hBN.

during film growth by creating localized defect states that interact strongly with deposited compounds and immobilize them.[60] The enhanced diffusion at the $CsSnI_3$/hBN interface facilitates crystal reorientation, enabling uniformly aligned nuclei to merge and form larger grains. XRD patterns of $CsSnI_3$ films grown on SiO_2 and hBN after 10 s of annealing displayed equally pronounced peaks in various orientations (Figure S4). In addition, stronger (101) orientation was observed from XRD patterns of $CsSnI_3$ film on SiO_2 substrates after 10 s of annealing, due to the rapid surface crystallization induced by dangling bonds. On the other hand, the (101) orientation in hBN counterparts was less evident at this stage, due to the initiation of crystallization at the film/substrate interface. However, after 10 min of annealing, the spectra of films on hBN exhibited a significant decrease in minor peaks compared with the SiO_2 counterparts (Figure 1f). The differences in variation in lattice orientations during thermal annealing suggest that perovskite crystals are localized at the dangling bonds of SiO_2, whereas on hBN, the perovskite crystals self-reorient along the (101) direction, promoting the merging of crystals and formation of larger grains.[61] We also investigated on whether chemical interaction occurs between $CsSnI_3$ layer and the underlying substrate and contributes to film growth and orientation. Through X-ray photoelectron spectroscopy (XPS) depth profiling of Sn 3d spectra for $CsSnI_3$ film on hBN and SiO_2 substrates, we observed that there was negligible difference between the film/substrate interface of the two samples (Figure S5). Thus, the decisive factor governing film growth on these two substrates is the physical interaction—namely, the hydrophobicity and absence of dangling bonds—rather than chemical interaction. Consequently, smaller grains with a higher density of defects, such as interfacial pinholes, are observed in $CsSnI_3$ films grown on substrates with dangling bonds like SiO_2. Thus, a dangling-bond-free and hydrophobic surface is essential for the formation of large crystals.

The interfacial trap densities of $CsSnI_3$ films on SiO_2 and hBN were calculated based on capacitance−voltage ($C-V$) measurements using a metal-oxide-semiconductor structure, applying the high-low method (Figure 4a). The $C-V$ curves of $CsSnI_3$ films grown on SiO_2 showed frequency dispersion owing to the high interfacial trap density, a behavior also observed in other semiconducting materials such as indium−gallium−zinc−oxide, III−V semiconductors, and perovskites.[62−64] The interfacial trap densities of $CsSnI_3$ films on

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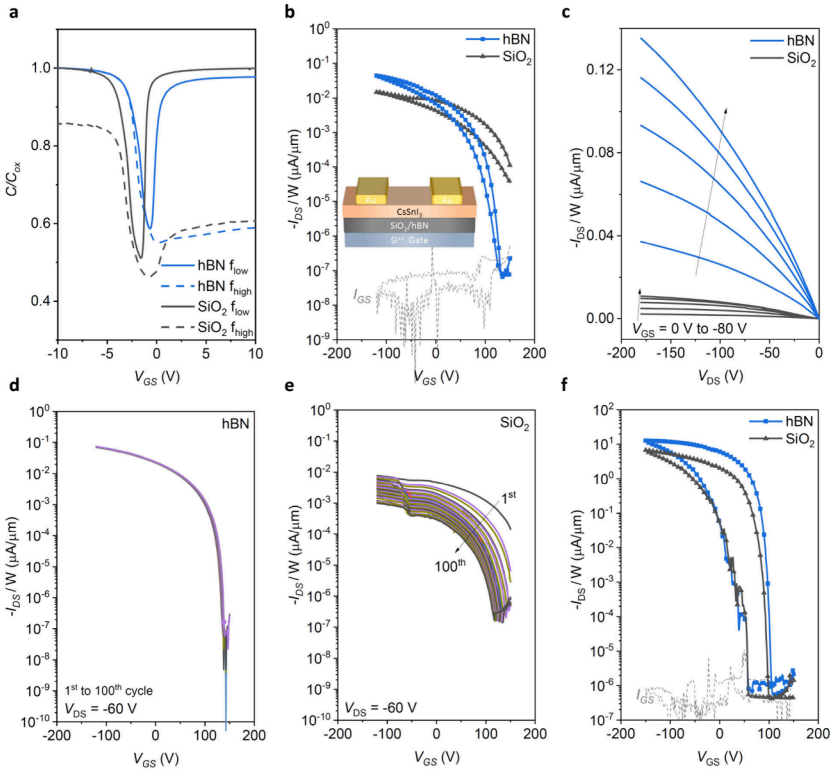

Figure 4. (a) Capacitance−voltage characteristics of $CsSnI_3$ films grown on SiO_2 and hBN in a metal-oxide-semiconductor structure. (b) Transfer characteristics of thin-film transistors (TFTs) based on $CsSnI_3$ films grown on SiO_2 and hBN. Channel length/width = 100 μm/1000 μm (V_{DS} = −60 V). (c) Corresponding output characteristics (ΔV_{GS} = −20 V). Results of 100-cycle test (d) on hBN and (e) on SiO_2 (V_{DS} = −60 V). (f) Transfer characteristics of $PbCl_2$-incorporated $CsSnI_3$ TFTs on SiO_2 and hBN. Channel length/width = 100 μm/200 μm (V_{DS} = −60 V).

SiO_2 and hBN were 5.22×10^{11} and 4.98×10^{10} cm^{-2} eV^{-1}, respectively (Figure S6). Moreover, the difference in oxide trap densities (ΔD_{ot}) based on flat-band voltage shifts of $CsSnI_3$ films grown on SiO_2 and hBN was 8.62×10^{10} cm^{-2} eV^{-1}. The larger interfacial trap density on SiO_2 was correlated with the smaller grain sizes and large pinholes observed in the cross-sectional SEM images.[65−67] Moreover, the introduction of the hBN monolayer on SiO_2 prevented carrier transport from being hindered by SiO_2 oxide traps.[68]

To verify the effect of the exceptionally high crystallinity and excellent interface characteristics of $CsSnI_3$ films grown on hBN on electrical properties, we fabricated bottom-gate, top-contact (BGTC) TFTs. Specifically, we deposited 10 nm $CsSnI_3$ films on SiO_2 and hBN without any hole-suppressor additives and annealing to avoid dewetting at elevated temperatures and ensure channel connectivity (Figure 4b, Figure S7). The $CsSnI_3$ TFT grown on SiO_2 displayed low current modulation with I_{on}/I_{off} of $(1.58 \pm 0.65) \times 10^2$ and I_{on}/W of 0.012 ± 0.005 μA μm^{-1}, whereas the $CsSnI_3$ TFT grown on hBN demonstrated a higher I_{on}/I_{off} of $(8.07 \pm 1.93) \times 10^6$, I_{on}/W of 0.067 ± 0.005 μA μm^{-1}, and linear mobility ($\mu_{FET, lin}$) of 0.117 ± 0.003 cm^2 V^{-1} s^{-1}. The output characteristics of $CsSnI_3$ TFTs grown on hBN displayed a higher magnitude of drain current compared with that of TFTs grown on SiO_2 (Figure 4c). In comparison to SiO_2 counterparts, the $CsSnI_3$ films on hBN displayed the reduction of pinholes and grain boundaries, regions in which V_{Sn} is highly concentrated, mitigating excessive self-p-doping of $CsSnI_3$ and enabling operating on/off current modulation without hole suppressors.[69,70] The hole concentrations of 10 nm $CsSnI_3$ films on hBN and SiO_2 were extracted by Hall measurement, which were $(1.11 \pm 0.47) \times 10^{17}$ cm^{-3} and $(1.16 \pm 0.14) \times 10^{18}$ cm^{-3}, respectively. The reduction in hole concentration down an order of a magnitude from $CsSnI_3$ film on SiO_2 to hBN, confirms the correlation between reduction of physical voids and self-p-doping to successful modulation of on/off current in TFT operation. The reduction of hole concentration with the use of hBN highlights a key distinction from previous approach using additives on SiO_2.[37] While the use of Cl-based additives required higher annealing temperatures (∼320 °C) for activating enhanced crystallization through vaporization of Cl-related species and thermal diffusion, the use of hBN enables additive-free crystallization with lower thermal barrier for effective diffusion, simplifying device fabrication. In addition, the operational stability of $CsSnI_3$ TFTs grown on SiO_2 and hBN was tested via 100-cycle transfer curve measurements. The TFTs on hBN demonstrated negligible degradation, whereas those on SiO_2 displayed decreasing on-current along with a negative shift in threshold voltage and visible kinks during operation (Figure 4d, e). The decrease in on-current over consecutive current−voltage (I−V) measurements indicated carrier trapping at the interfacial traps and decrease in hole carriers participating in carrier transport.[71−74] The visible kinks at V_{GS} = −60 V were attributable to the trap-and-release phenomenon of charge carriers at deep trap levels.[75] Using the conductance method, the interfacial trap densities (D_{it}) of $CsSnI_3$ TFTs grown on SiO_2 and hBN were calculated to be 3.20×10^{12} and 1.84×10^{12} cm^{-2} eV^{-1}, respectively (Figure S8).

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The influence of hBN on $CsSnI_3$ film growth with the incorporation of $PbCl_2$, a hole suppressor and crystallinity enhancer, on a thicker film (40 nm) was examined.[37] The effect of $PbCl_2$, driven by Cl-related vaporization, was also effective on hBN. Specifically, the $CsSnI_3$:$PbCl_2$ BGTC TFTs on hBN displayed a higher I_{on}/I_{off} of $(2.14 \pm 0.56) \times 10^7$, I_{on}/W of 13.5 ± 0.4 $\mu A\ \mu m^{-1}$, and saturation mobility ($\mu_{FET,\ sat}$) of 23.7 ± 1.43 $cm^2\ V^{-1}\ s^{-1}$, higher than that of the SiO_2 counterparts ($(1.77 \pm 0.35) \times 10^7$, 6.457 ± 0.740 $\mu A\ \mu m^{-1}$, 8.46 ± 1.31 $cm^2\ V^{-1}\ s^{-1}$, respectively) (Figure 4f). The output characteristics of $CsSnI_3$:$PbCl_2$ TFTs on hBN also displayed higher drain currents than those on SiO_2 (Figure S9a). In addition, the $PbCl_2$-incorporated devices exhibited slightly lower turn-on voltages than undoped $CsSnI_3$ TFTs, which aligns with their reduced hole concentration. The operational stability of $CsSnI_3$:$PbCl_2$ TFTs exhibited greater improvement on hBN than on SiO_2, as observed in consecutive on/off switching tests over 1000 s. The TFTs on hBN displayed reduced performance degradation (Figure S9b). Overall, the growth of $CsSnI_3$-based channel layers on hBN significantly reduced grain boundaries and pinholes, modulating the intrinsic hole concentration and interfacial trap density and facilitating hole transport.

In conclusion, highly crystalline 3D $CsSnI_3$ films were successfully grown on dangling-bond-free and hydrophobic hBN surfaces via thermal evaporation. The introduction of hBN enhanced the quality of perovskite film by reducing the density of nucleation sites and increasing the nuclei size, resulting in enlarged grains. Moreover, hBN enhanced the quality of the semiconductor−dielectric interface by promoting the diffusion of precursor compounds during thermal treatment, thereby reducing interfacial trap densities. The $CsSnI_3$ films grown on hBN displayed reduced grain boundaries, where V_{Sn} is typically concentrated. TFTs adopting the resulting $CsSnI_3$ films on hBN as a channel layer exhibited on/off current modulation without hole-suppressing additives. This study provides valuable insights into the growth of high-quality 3D halide perovskite film by thermal evaporation, establishing a foundation for the commercialization of high-performance large-area perovskite circuits.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsenergylett.5c02309.

Experimental section (including monolayer hBN substrate synthesis and characterization, thin film fabrication and characterization, device fabrication and characterization, SIMS analysis); MSD & diffusion coefficient calculation; Mobility calculation; EBSD IPF image; EBSD pole figure image; SIMS image; XRD patterns; interface trap density; SEM images; conductance method; output curve; consecutive on/off switching curve; Raman spectrum (PDF)

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[⊥]T.R. and Y.R. contributed equally. R.-H.B., C.-J.K., and Y.-Y.N. conceived the study. T.R. and Y.R. performed the experiments. W.Y., G.P., J.-H.J., and S.-H.B. assisted in the device fabrication. B.H., J.A., S.H., and T.R. analyzed the data. T.R. prepared the manuscript draft. Y.R. and Y.Y.N. revised and finalized the manuscript. All authors contributed to the final version of this manuscript.

Notes

The authors declare no competing financial interest.

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